**Assignment**

**COEN 311**

**Computer Organization and Software**

**Assignment #2**

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“I certify that this submission is my original work and meets the

Faculty’s Expectations of Originality”

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# Short answer questions

## Question 1



Each memory segment is 64KB.

## Question 2



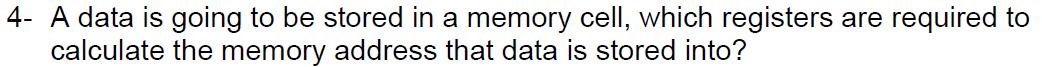
The instruction pointer stores the offset address, with respect to the code segment, of the next instruction in memory to be executed.

## Question 3



To form the physical address, we add the base address, shifted to the left by 4 bits, with the offset address.

## Question 4



To calculate the memory address that we’ll store the data in, we use the data segment register (DS) to get the base address.

## Question 5



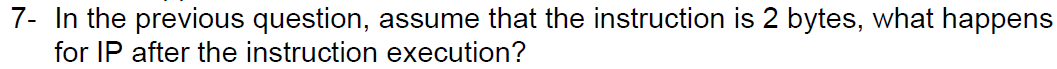
Address/Memory locations are stored in pointer and index registers.

## Question 6



The instruction pointer is incremented by the size of the instruction that was executed. This places its current value at the location of the next instruction to execute.

## Question 7



IP = IP+0002

## Question 8



The segment registers hold the lowest/base address of a segment.

## Question 9

Text

Description automatically generated

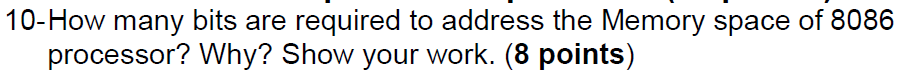
Von-Neuman architecture since we only have 1 memory bus.

~~Harvard architecture since memory is broken up into segments meaning we have a section for data memory (the data segment) and a section for instruction memory (the code segment). These segments can be used individually.~~

Its also a CISC because its instruction set is simpler. One instruction can perform multiple operations with only one instruction.

# Computational Questions

## Question 10



Since the 8086 processor can have a memory capacity of 1Mb and it is byte organized,

bits are required to address the memory space

## Question 11

Text

Description automatically generated

Shift the base address to the left by 4 bits, then add the offset address to get the physical address.

a)  
Base Address: 1000 shifted by 4 bits 10000

Offset address: 1234



**Physical address: $11234**

b)

Base Address: 0100 shifted by 4 bits 01000

Offset address: ABCD



**Physical Address: $0BBCD**

c)

Base Address: A200 shifted by 4 bits A2000

Offset address: 12CF



**Physical Address: $A32CF**

## Question 12

Text

Description automatically generated

a)

Physical Address: A0123

Base Address: A000 shifted by 4 bits A0000



Offset Address: **$0123**

b)

Offset address: 14DA

Physical Address: 235DA



**Base Address: $2210**

c)

Physical Address: DABC0

Base Address: D765 shifted by 4 bits D7650



**Offset Address: $3570**

# Addressing Mode Questions

## Question 13

Text

Description automatically generated with medium confidence

a)

Source: register mode

Destination: register mode

b)

Source: immediate

Destination: register mode

c)

Source: register mode

Destination: indexed

d)

Source: indexed mode

Destination: register mode

e)

Source: register mode

Destination: based mode

## Question 14

Text

Description automatically generated

a)

Base Address is DS: $0B00 shifted by 4 bits$0B000

Offset Address: $0200



**Physical Address: $0B200**

b)

Base Address is DS: $0B00 shifted by 4 bits$0B000

Offset Address: $0100



**Physical Address: $0B100**

c)

Base Address is DS: $0B00 shifted by 4 bits$0B000

Offset: $0300 + $0400 = $0700



**Physical Address: $0B700**